**Verification of Lab 4 Part A**

**EE 316 Spring 2020**

**Last edited by Mertcan Temel on 03/20/20**

This document includes instructions for you to run a comprehensive test for your module for Lab 4 Part A. A script is prepared specifically for this lab using the formal verification tool ACL2, and it is set up on UT ECE virtual machines. When you follow these instructions, you can get a more easily interpretable result than simulation on Vivado.

This is an optional document (for this lab); however, you are strongly encouraged to test your design with this tool. You will feel more confident that your code is working, and you may add these results to your submission as a proof of correctness. We will follow a very similar procedure for the last two labs, which will then be mandatory. So, try to get acquainted now.

Before you try this tool, make sure your code can synthesize in Vivado, and it seems to be working in simulation.

**Testing your code for correctness:**

1. Connect to University of Texas VPN: <https://vpn.utexas.edu/>
2. Upload your “clks.v” anywhere in your directory in UT ECE machines. You may use an FTP program such as Filezilla.
3. Using a terminal (e.g., Putty or Mobaxterm if you are using Windows), ssh to an ECE virtual machine (<http://www.ece.utexas.edu/it/virtual-linux-resources>)
4. Navigate to the directory where your “clks.v” is located. Your file has to be named “clks.v” and your module’s name should be clks with the port declarations given in the manual. It is also assumed that you only use rising\_edge of the input clock.
5. Run the below command. This will create an alias for the current session.

|  |
| --- |
| alias lab4atest="/home/ecelrc/students/mtemel/ee316/lab4-parta-test" |

1. Then run:

|  |
| --- |
| lab4atest |

This will test your code using a formal verification tool called ACL2. UT ECE machines allocate very little resources for each student, and this may take 5-10 minutes to run. However, it will tell you definitely whether or not your code is correct. If it is not, it will throw an error message.

**Interpreting the output:**

* If your design is correct, you will see a prompt message as seen below:

A screenshot of a cell phone

Description automatically generated

If you see the line that starts with “Built”, it means your design is correct. If you want to submit a proof for correctness (you are encouraged to do so), take a screenshot such as this one and include it in your submission.

* If your design is not correct, a very long error message will be printed that looks like the one below:

A screenshot of a cell phone

Description automatically generated

Pay attention to the line that starts with HARD ACL2 ERROR. It tells you which output frequency does not match the specification. Above that, it also tells you the calculated frequencies for all your outputs. Compare with the target (specification) frequencies and fix your design accordingly.

* If one of your output does not generate a clock or if it is very slow, then you will see “-1” for calculated frequencies.
* Some UT ECE machines load older versions of some required libraries. If you get an error that says “’GLIBC\_2.14' not found”, try other machines. The machines we know to work are mario, wario, bowser, daisy and yoshi. On the other hand, kamek, koopa and luigi fail to work.
* If you encounter any other error and you are not sure how to interpret, please use Piazza to ask your questions for everyone to see.